Notice of Allowability	Application No.	Applicant(s)	
	10/574,120	BRUEL, MICHEL	
	Examiner	Art Unit	
	ATUL P. KHARE	1742	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Examiner-initiated interview on 9/15/11*.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are *34-36,38 and 40-55*.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☒ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 9/15/11
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *9/15/11* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/ATUL P. KHARE/
Examiner, Art Unit 1742

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Allan A. Fanucci on 15 September 2011.

The application has been amended as follows:

Claim 34: (Currently Amended) A method for fabricating a **silicon wafer,** [~~structure in the form of a plate~~] which method comprises:

depositing at least one intermediate layer on either of a substrate and/or a superstrate **by chemical vapor deposition,** wherein the intermediate layer **is deposited as a glass comprising** [~~comprises~~] at least one base material having distributed therein extrinsic atoms or molecules which differ from those of the base material;

assembling the substrate and the superstrate so that the **as-deposited** intermediate layer is interposed between the substrate and the superstrate to form a **silicon wafer** structure[~~,~~]; and

applying a heat treatment to the **resulting** structure in a temperature range that causes the intermediate layer to become **spongy and** plastically deformable with the

as-deposited extrinsic atoms or molecules in the base material causing an irreversible formation of microbubbles or microcavities in the intermediate layer **resulting from the heat treatment** in a configuration and amount [~~sufficient to~~] **which** weaken**s** the intermediate layer.

Claim 36: (Currently Amended) The method as claimed in claim 34, which further comprises applying forces between the substrate and the superstrate to bring about the rupture of the intermediate layer between the substrate and the superstrate due to the presence of the **microbubbles** [~~micro-bubbles~~] or **microcavities** [~~micro-cavities~~].

Claim 39: (Canceled)

Claim 41: (Currently Amended) The method as claimed in claim 34, wherein[~~,~~] after the heat treatment, at least some **of** the microbubbles or microcavities have a volume such that they are open both on the substrate and on **the** superstrate side**,** or furthermore **that they** are mutually open to constitute channels which are open between the side ends of the intermediate layer.

Claim 43: (Currently Amended) The method as claimed in claim 41, which further comprises cooling the structure by circulating a cooling fluid through the channels formed by the **microbubbles** [~~micro-bubbles~~] or **microcavities** [~~micro-cavities~~].

Claim 48: (Currently Amended) The method as claimed in claim 54, wherein the concentration of phosphorus is in the range from 6% to 14% [~~or the concentration of boron is in the range from 0% to 4%~~].

Claim 52: (Currently Amended) The method as claimed in claim 50, which further comprises, prior to the step of depositing, providing a thermal silicon oxide on each of the substrate and superstrate[~~,~~] so that the intermediate layer is deposited on the thermal silicon oxide on either of the substrate or the superstrate.

Claim 54: (Currently Amended) The method as claimed in claim 47**,** wherein **the** extrinsic atoms further comprise atoms of boron, thus forming an intermediate layer of boro-phospho-silicate glass**.**

Claim 55: (New) The method as claimed in claim 54, wherein the concentration of boron is in the range from 0% to 4%.

2. The following is an examiner's statement of reasons for allowance: The closest prior art of record teaches (1) forming a weakened intermediate layer by gas/ion implantation and then heat treatment, or (2) depositing a porous intermediate layer of silicon (see below). Regarding (1) and (2), the intermediate layer can be disposed between a substrate and superstrate for separation at the intermediate layer by the application of thermal, mechanical, or chemical forces. Regarding (2), the closest prior

art of record suggests (a) using a doped intermediate layer, and (b) using heat treatment to weaken the intermediate layer. However, the prior art of record does not teach, suggest, or disclose fabricating a silicon wafer by depositing an intermediate layer onto a substrate and/or superstrate, assembling the substrate and superstrate with the as-deposited intermediate layer disposed therebetween, and applying a heat treatment to the resulting structure to cause the intermediate layer to become spongy and plastically deformable, wherein the intermediate layer is deposited as a glass, and wherein extrinsic atoms or molecules in the intermediate layer cause an irreversible formation of microbubbles or microcavities resulting from said heat treatment.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Aspar (US 7,713,369), Chu (US 6,774,010), Tayanaka (US 6,759,310), Sakaguchi (US 6,426,270), Sakaguchi (US 2002/0048844), and Hashimoto (US 5,817,368) teach forming a porous silicon intermediate layer between a silicon substrate and superstrate, wherein the porous layer can be used to separate the substrate and superstrate. Usenko (US 6,352,909) teaches forming a buried intermediate separating layer by gas/ion implantation.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to ATUL P. KHARE whose telephone number is (571)270-7608. The examiner can normally be reached on Monday-Thursday 7:30 a.m. - 5:00 p.m. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Christina Johnson can be reached on (571)272-1176. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/ATUL P. KHARE/
Examiner, Art Unit 1742

/Christina Johnson/

Supervisory Patent Examiner, Art Unit 1742